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APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Cheolsoo Park, a citizen of Republic of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Republic of Korea have invented a new and useful **METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method for manufacturing a fine transistor having a size less than 0.10 μm.

BACKGROUND

In general, as a semiconductor device becomes highly integrated, approaches for realizing a nano-technology in a manufacturing of the semiconductor device have been developed. However, a tool or a material of lithography using, particularly, a deep ultraviolet (DUV) equipment, is recently insufficient in view of a mass production and thus a size of a diameter of a wafer is enlarged. In addition, the purchase cost of the tool and a process costs are excessively increased.

For example, United States Patent No. 6,346,467 discloses a method of making tungsten gate MOS transistor and memory cell by encapsulation and U.S. Patent Application Publication No. US2002/0001935 A1 discloses a method of forming a gate electrode in a semiconductor device which can prevent transformation of the gate electrode.

However, in such examples, when a fine transistor having a size of not greater than 0.10 μm is manufactured, there are limitations and drawbacks in forming a gate electrode having a small critical dimension. Particularly, as the critical dimension of the gate electrode is reduced, a short channel effect, in which a threshold voltage

becomes small due to a shorter length between a source channel and a drain channel, occurs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Figs. Figs. 1A to 1D represent an example process for manufacturing a fine transistor.

DETAILED DESCRIPTION

[0003] As described in greater detail below, a fine transistor having a size of not greater than 0.10 μm is fabricated by forming a doped poly silicon layer for controlling a length of a gate channel in a formation of a gate and reducing a cost of a lithography tool. In one example, a method for fabricating a transistor in a semiconductor device forms an isolation region in a semiconductor substrate and sequentially deposits a pad oxide layer, a pad nitride layer and a first oxide layer on the substrate and the isolation region. The example method also patterns the first oxide layer and pad nitride layer to form a gate electrode, deposits a doped poly silicon layer, and forms a doped polysilicon sidewall on the pad nitride layer and first oxide layer. In addition, the example method etches the pad oxide layer, sequentially deposits and planarizes a gate isolation layer, a gate nitride layer and a metal layer on the substrate to thereby form the gate electrode, and forms a source, a drain, a gate plug, a source plug and a drain plug, respectively.

[0004] Figs. 1A to 1D represent an example procedure for manufacturing a fine transistor. Referring to Fig. 1A, a shallow trench isolation (STI) 20 is formed in a silicon substrate 10. A pad oxide layer 30, a pad nitride layer 40 and a first oxide layer 50 are sequentially deposited on the substrate 10. A thickness of the first oxide layer 50 is about equal to that of a gate electrode to be formed later.

[0005] Referring to Fig. 1B, a photoresist 60 on the first oxide 50 is patterned in order to be used in forming the gate electrode. Next, the first oxide layer 50 and the pad nitride layer 40 are sequentially dry etched. The pad oxide layer 30 has a thickness of at least 50 angstrom.

[0006] Referring to Fig. 1C, a cleaning is performed after removing the photoresist 60. Next, a doped poly silicon layer is deposited all over the pad oxide layer 30, the pad nitride layer 40 and the first oxide layer 50, and the doped poly silicon layer is etched back to expose the pad oxide layer 30 to thereby form a doped poly silicon sidewall 70 on a sidewall of the pad nitride layer 40 and the first oxide layer 50.

[0007] Next, the pad oxide layer 30 exposed by the doped poly silicon sidewall 70 is removed using a precleaning method to expose the silicon substrate 10, and then a gate isolation layer 80 is formed on the silicon substrate 10. The thickness of the gate isolation layer 80 is preferably smaller than that of the pad oxide layer 30. A gate nitride layer 90 of, e.g., TiN or TaN, is deposited by a chemical vapor deposition (CVD) covering the gate isolation layer 80 and the doped polysilicon sidewall 70, and a metal layer 100 of, e.g., tungsten (W) is filled and thickly deposited thereon. A CMP process is performed to thereby form the gate electrode.

[0008] A local channel ion implantation is performed only in case a source and a drain region are salicidated or a lightly doped drain (LDD) implantation is performed before the gate isolation layer 80 is deposited.

[0009] In one example, the doped poly silicon sidewall 70 may be used to function as the LDD implantation without forming the LDD implantation. In other words, when a power is applied to the gate electrode, the pad oxide layer 30 under the doped poly silicon sidewall 70 may serve as an LDD doping role by controlling the thickness of the pad oxide layer 30 under the doped poly silicon sidewall 70 because the pad

oxide layer 30 under the doped poly silicon sidewall 70 is thicker than the gate isolation layer 80.

[0010] Referring to Fig. 1D, the first oxide layer 50 is removed using a wet etching or a dry etching, and a source and a drain are formed by an ion implantation. Thereafter, a first insulation layer 110 is thickly deposited and then planarized using a CMP. Finally, a gate plug 120A, a source plug 120b and a drain plug 120c are formed.

[0011] In accordance one example, the gate having a fine pattern can be formed by using the doped poly silicon sidewall 70 for use in controlling the channel length of the gate so that it can be obtained a new method capable of enhancing an operating characteristic of a transistor and reducing a cost of a lithography tool. Also, the thickness of the pad oxide layer 30 under the doped poly silicon sidewall 70 can be controlled so that the LDD implantation may be substituted with the pad oxide layer 30 under the doped poly silicon sidewall 70.

[0012] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.